REMARKS

The allowance of claims 2, 3, 5 and 6 is gratefully acknowledged by the applicant. The statement that claim 4 contains allowable subject matter is also gratefully acknowledged.

Claims 1 and 4 have been amended. Claims 1-6 are presently pending, of which claims 2, 3, 5 and 6 have been allowed. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claim 4 stands objected to based on informalities. Claim 4 has been amended, in accordance with the Examiner's recommendations, to overcome this objection. The objection is respectfully traversed. Accordingly, Applicant respectfully requests that the objection be withdrawn and claim 4 allowed.

Claim 1 stands rejected under 35 U.S.C 102(b) as being anticipated by Saito, U.S. Patent No. 5,377,178. The rejection is respectfully traversed.

Claim 1 recites a "data recording clock signal generator that generates a recording clock signal synchronous with a wobble signal used for recording data on an optical disk." The generator includes a recording clock signal generating unit that generates the recording clock signal having a frequency controlled in accordance with the frequency control signal generated by the frequency control signal generator. The recording clock signal dividing unit is provided with a "a frequency dividing rate setting unit that sets in accordance with predetermined procedures, a reference frequency dividing rate and a frequency dividing rate different from the reference frequency dividing rate by which the frequency of the recording clock signal is divided." According to claim 1, "a time period, over which the frequency dividing rate different from the reference frequency dividing rate is set, is set shorter than an operating time constant of the frequency dividing rate setting unit." Applicant respectfully submits that Saito fails to disclose the claim 1 invention.

That is, Saito fails to disclose a time period that is set shorter than the frequency of the time constant of the dividing rate setting unit. In Saito, the frequency dividing rate is changed in accordance with the zone number Nz, as described in col. 20, lines 60-66 and col. 21, lines 4-10. Thus, the Saito changing rate of the frequency dividing rate is low, as opposed to the time period that is shorter than the operating time constant in the claimed invention. Although Saito indicates that realignment occurs when a misalignment is detected, Saito fails to disclose the method by which the realignment will occur and further fails to disclose the use of a time period that is less than the time constant. Additionally, the Saito fails to describe a frequency dividing rate change that is not made in accordance with the zone number Nz. As such, claim 1 is allowable over Saito.

Furthermore, Saito fails to disclose that a motor control circuit sets a reference frequency dividing rate and another frequency dividing rate in accordance with predetermined procedures. This is one more reason why claim 1 is patentable over Saito.

The rejection should be withdrawn and claim 1 allowed.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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